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1 Session S4.1: power in memory and network processors: Embedded cache architecture with programmable write buffer support for power and performance flexibility
Afzal Malik, Bill Moyer, Roger Zhou
October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(122.19 KB) Additional Information: full citation, abstract, references, index terms

Next generation portable devices are placing stringent requirements on overall system power and performance. Voice recognition, streaming video and high speed wire¿less internet access are just some of the features being incorporated in these handheld electronic gadgets. The M¿CORE M341-S processor has been designed for high performance and cost sensitive portable products as well as for high end embedded control applications. M341-S obtains increased performance over the M¿CORE M2 and M310 fami ...

Keywords: cache control, cache management, copyback, programmable, push buffer, write buffer, writethrough

2 Dynamic voltage scaling for real-time multi-task scheduling using buffers
Chaeseok Im, Soonhoi Ha
June 2004 **ACM SIGPLAN Notices , Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools**, Volume 39 Issue 7
Full text available: pdf(335.31 KB) Additional Information: full citation, abstract, references, index terms

This paper proposes energy efficient real-time multi-task scheduling (EDF and RM) algorithms by using buffers. The buffering technique overcomes a drawback of previous approaches by utilizing the slack time of a system fully. It increases the CPU utilization and averages the workload of a system, so it enhances the effectiveness of the DVS technique. We target multimedia applications where a slight buffering delay is tolerable within a latency constraint. We modify the state transition and queue ...

Keywords: dynamic voltage scaling, real-time systems, scheduling

3 Power grid design and analysis techniques: Buffer sizing for clock power minimization subject to general skew constraints
Kai Wang, Malgorzata Marek-Sadowska

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(193.65 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we investigate the problem of buffer sizing for clock power minimization subject to general skew constraints. A novel approach based on sequential linear programming is presented. By taking the first-order Taylor's expansion of clock path delay with respect to buffer widths, the original nonlinear problem is transformed to a sequence of linear programs, which incorporate clock skew scheduling and buffer sizing to minimize clock power dissipation. For each linear program, the sensi ...

Keywords: clock skew scheduling, sequential linear programming, sizing

4 Clock routing and buffering: Fast and flexible buffer trees that navigate the physical layout environment

Charles J. Alpert, Milos Hrkic, Jiang Hu, Stephen T. Quay

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(400.02 KB) Additional Information: full citation, abstract, references, index terms

Buffer insertion is an increasingly critical optimization for achieving timing closure, and the number of buffers required increases significantly with technology migration. It is imperative for an automated buffer insertion algorithm to be able to efficiently optimize tens of thousands of nets. One must also be able to effectively navigate the existing layout, including handling large blockages, blockages with holes specifically for buffers, specially allocated buffer blocks, placement porosity ...

Keywords: buffer insertion, global routing, physical synthesis

5 An approximate analysis of the LRU and FIFO buffer replacement schemes

Asit Dan, Don Towsley

April 1990 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 18 Issue 1

Full text available: pdf(956.70 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we develop approximate analytical models for predicting the buffer hit probability under the Least Recently Used (LRU) and First In First Out (FIFO) buffer replacement policies under the independent reference model. In the case of the analysis of the LRU policy, the computational complexity for estimating the buffer hit probability is O (KB) where B is the size of the buffer and K denotes the number of items h ...

6 The accumulation buffer: hardware support for high-quality rendering

Paul Haeberli, Kurt Akeley

September 1990 **ACM SIGGRAPH Computer Graphics , Proceedings of the 17th annual conference on Computer graphics and interactive techniques**, Volume 24 Issue 4

Full text available: pdf(3.46 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a system architecture that supports realtime generation of complex images, efficient generation of extremely high-quality images, and a smooth trade-off between the two.Based on the paradigm of integration, the architecture extends a state-of-the-art rendering system with an additional high-precision image buffer. This additional buffer, called the Accumulation Buffer, is used to integrate images that are rendered into the framebuffer. While originally conceived as a solutio ...

7 Rendering CSG models with a ZZ-buffer

David Salesin, Jorge Stolfi

September 1990 **ACM SIGGRAPH Computer Graphics , Proceedings of the 17th annual conference on Computer graphics and interactive techniques**, Volume 24 Issue 4

Full text available: pdf(2.32 MB) Additional Information: full citation, abstract, references, citings, index terms

The ZZ-buffer is a simple acceleration scheme for ray tracing that can be applied to a wide variety of scenes, including those with small features, textured and transparent surfaces, shadows and penumbrae, and depth-of-field effects. In this paper, we describe how the ZZ-buffer algorithm can be adapted to the rendering of scenes defined by constructive solid geometry operations.

8 Applications: Repairing return address stack for buffer overflow protection

Yong-Joon Park, Gyungho Lee

April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: pdf(197.90 KB) Additional Information: full citation, abstract, references, index terms

Although many defense mechanisms against buffer overflow attacks have been proposed, buffer overflow vulnerability in software is still one of the most prevalent vulnerabilities exploited. This paper proposes a micro-architecture based defense mechanism against buffer overflow attacks. As buffer overflow attack leads to a compromised return address, our approach is to provide a software transparent micro-architectural support for return address integrity checking. By keeping an uncompromised cop ...

Keywords: buffer overflow, computer architecture, computer security, intrusion tolerance

9 Routing topology optimization: A fast algorithm for identifying good buffer insertion candidate locations

Charles J. Alpert, Milos Hrkic, Stephen T. Quay

April 2004 **Proceedings of the 2004 international symposium on Physical design**

Full text available: pdf(340.92 KB) Additional Information: full citation, abstract, references, index terms

Van Ginneken's algorithm [18] for performing buffer insertion is a classic in the field, since it optimally solves the problem subject to a set of fixed buffer insertion candidate locations for a given Steiner topology. The generation of these candidate locations is typically performed by dividing the routed wires into small uniformly sized pieces [1]. However, certain regions of the layout are generally more attractive to place buffers than others, e.g., sparse regions are preferred to dense on ...

Keywords: buffer insertion, global routing, physical synthesis, planning

10 Analysis and verification: Buffer overrun detection using linear programming and static analysis

Vinod Ganapathy, Somesh Jha, David Chandler, David Melski, David Vitek

October 2003 **Proceedings of the 10th ACM conference on Computer and communication security**

Full text available: pdf(196.29 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the issue of identifying buffer overrun vulnerabilities by statically analyzing C source code. We demonstrate a light-weight analysis based on modeling C

string manipulations as a linear program. We also present fast, scalable solvers based on linear programming, and demonstrate techniques to make the program analysis context sensitive. Based on these techniques, we built a prototype and used it to identify several vulnerabilities in popular security critical applications.

Keywords: buffer overruns, linear programming, static analysis

11 Floorplan Evaluation with Timing-Driven Global Wireplanning, Pin Assignment and Buffer/Wire Sizing

Christoph Albrecht, Andrew B. Kahng, Ion Mandoiu, Alexander Zelikovsky

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(270.36 KB) Publisher Site Additional Information: full citation, abstract

We describe a new algorithm for floorplan evaluation using timing-driven buffered routing according to a prescribed buffer site map. Specifically, we describe a provably good multi-commodity flow based algorithm that finds a global routing minimizing routing area (wirelength and number of buffers) subject to given constraints on buffer/wire congestion and sink delays. This permits detailed floorplan evaluation, i.e., computing the tradeoff curve between routing area and wire/buffer congestion un ...

12 High-speed buffering for variable length operands

H. L. Tredennick, T. A. Welch

March 1977 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th annual symposium on Computer architecture**, Volume 5 Issue 7

Full text available: pdf(501.08 KB) Additional Information: full citation, abstract, references, citings, index terms

Variable word length processing is valuable for data base manipulations, editing functions in time-sharing systems, input-output data formatting, and vector operations, but current computer architectures seldom provide efficient means for manipulating variable length operands. A specialized computer architecture has been proposed to deal with the problems of variable length byte string processing. Operand buffering is a key part of the proposed architecture because the buffer: (1) replaces ...

13 I/O buffer performance in a virtual memory system

Stephen W. Sherman, Richard S. Brice

August 1976 **Proceedings of the fourth symposium on Simulation of computer systems**

Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, index terms

In this study we construct a simulator of a data base management system running in a virtual memory environment. We use the simulator to investigate the value of using an I/O buffer in this environment. The simulator is driven by trace data obtained with a software probe. The simulator is validated and is used to verify a theoretical model which predicts paging and disk access rates produced by use of an I/O buffer in a virtual memory environment. Results from a multi-factor set of simulati ...

14 Can message buffers be characterized in linear temporal logic?

A. P. Sistla, E. M. Clarke, N. Francez, Y. Gurevich

August 1982 **Proceedings of the first ACM SIGACT-SIGOPS symposium on Principles of distributed computing**

Full text available: pdf(577.60 KB) Additional Information: full citation, abstract, references, citings, index terms

Exchange of information between executing processes is one of the primary reasons for process interaction. Many distributed systems implement explicit message passing primitives to facilitate intercommunication. Typically, a process executes a write command to pass a message to another process, and the target process accepts the message by executing a read command. The semantics of write and read may differ considerably dep ...

15 Configuring buffer pools in DB2 UDB

Xiaoyi Xu, Patrick Martin, Wendy Powley

September 2002 **Proceedings of the 2002 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(96.74 KB) Additional Information: full citation, abstract, references, citings, index terms

Database Management Systems (DBMSs) use a main memory area as a buffer to reduce the number of disk accesses performed by a transaction. DB2 Universal Database divides the buffer area into a number of independent buffer pools and each database object (table or index) is assigned to a specific buffer pool. The tasks of configuring the buffer pools, which defines the mapping of database objects to buffer pools and setting a size for each of the buffer pools, is crucial for achieving optimal perfor ...

16 An analytical model for buffer hit rate prediction

Yongli Xi, Patrick Martin, Wendy Powley

November 2001 **Proceedings of the 2001 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(100.79 KB) Additional Information: full citation, abstract, references, index terms

Of the many tuning parameters available in a database management system (DBMS), one of the most crucial to performance is the buffer pool size. Choosing an appropriate size, however, can be a difficult task. In this paper we present an analytical modeling approach to predicting the buffer pool hit rate that can be used to simplify the process of buffer pool sizing. A Markov Chain model is used to estimate the hit rate for buffer pools in IBM's DB2 Universal Database. We present and experimental ...

17 Pipelines with internal buffers

Janak H. Patel

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

Full text available: pdf(508.00 KB) Additional Information: full citation, abstract, references, citings, index terms

Concurrent or overlapped processing of more than one task is a common technique used in many computer architectures to increase the throughput. A pipeline is one such form consisting of a set of hardware segments which can be operated in an overlapped fashion. The existing and many proposed pipelines assume that a task must flow synchronously, without wait or preemption, from segment to segment for its execution. In this paper we propose a pipeline model in which priority buffers are provid ...

18 On the effectiveness of buffered and multiple arm disks

Alan Jay Smith

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

Full text available: pdf(662.74 KB) Additional Information: full citation, abstract, references, citings, index terms

Access patterns to input/output files are usually sequential and local; a small number of files are open for each job and the file is generally read or written sequentially. This implies that if files are allocated in contiguous disk storage, the disk arms will rarely be required to move. Disk seeks can be almost entirely eliminated by using multiple arms, whereby if

there are several open files on a given spindle, there will be an arm for each. Even better results can be obtained by using ...

19 On updating buffer allocation

Ashok K. Thareja, Satish K. Tripathi, Richard A. Upton

April 1982 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the Computer Network Performance Symposium**, Volume 11 Issue 1

Full text available: pdf(528.33 KB) Additional Information: full citation, abstract, references, index terms

Most of the analysis of buffer sharing schemes has been aimed at obtaining the optimal operational parameters under stationary load situations. It is well known that in most operating environments the traffic load changes. In this paper, we address the problem of updating buffer allocation as the traffic load at a network node changes. We investigate the behavior of a complete partitioning buffer sharing scheme to gain insight into the dependency of the throughput upon system parameters. Th ...

20 Floorplanning and placement: Dynamic global buffer planning optimization based on detail block locating and congestion analysis

Yuchun Ma, Xianlong Hong, Sheqin Dong, Song Chen, Yici Cai, C. K. Cheng, Jun Gu

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(205.60 KB) Additional Information: full citation, abstract, references, citings, index terms

By dividing the packing area into routing tiles, we can give the budget of the buffer insertion. And the detail locating of the blocks in their rooms can be implemented for each iterations during the annealing process to favor the later buffer planning. The buffer insertion will affect the possible routes as well the congestion of the packing. The congestion estimation in this paper takes the buffer insertion into account. So we devise a buffer planning algorithm to allocate the buffer into tile ...

Keywords: buffer insertion, congestion, floorplanning, routability

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- Enclose a phrase in double quotes to search for that exact phrase.

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